MachXO™: Optimized Programmable Devices for Bus Interfaces, Bridges and Control

A Lattice Semiconductor White Paper

July 2005

Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

Requirements for Bus Bridging, Interfacing and Control

Bus bridging, interfacing and control are common functions in many electronic systems. The use of these functions spans virtually every end market segment, including automotive, consumer, communications, computing, industrial and military. In many cases, designers turn to programmable logic devices, either low-capacity FPGAs or high-capacity CPLDs, to implement these functions. However, neither class of programmable logic device has offered an optimal solution that fully addresses the requirements for devices implementing these functions, including:

- High pin-to-pin speeds to meet critical bus timings
- Instant-on to allow control logic to function ahead of other devices
- Upgradeability to allow for field upgrades
- High I/O to logic ratio to address multiple wide busses
- Flexible capabilities for data buffering
- Low power

Traditional CPLD and FPGA Approaches

The CPLD architectural approach traditionally taken has been to build logic from Macrocells. Each Macrocell ORs together several wide (typically over 30 input) AND terms that are referred to as Product Terms. Historically, this approach has allowed fast wide logic to be implemented with a relatively simple set of design tools. In addition, CPLDs typically have been implemented using non-volatile technology, enabling the logic to be available instantly on power-up, a feature known as “instant-on.” In contrast, the FPGA architectural approach constructs logic out of 4-input Look-Up Tables (LUTs). Figure 1 compares the two approaches.

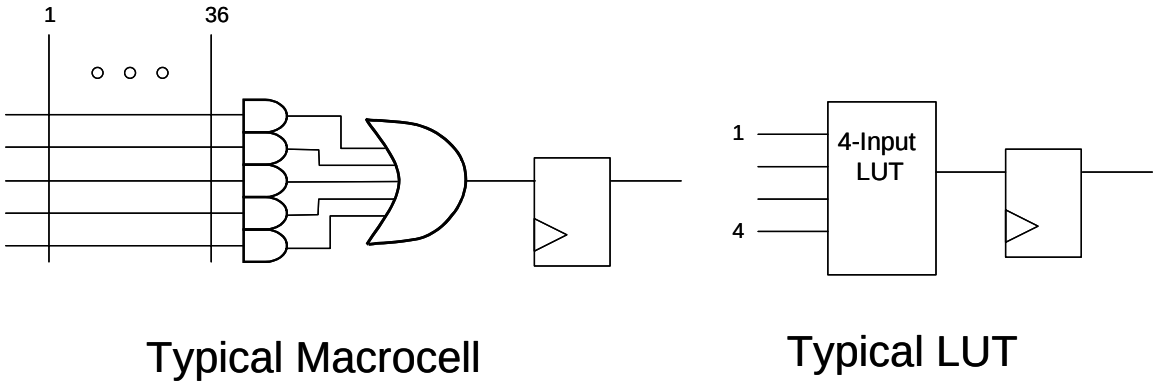


Figure 1 – CPLD Macrocell and FPGA LUT Elements

The LUT approach is flexible, but requires functions of many inputs to be constructed from multiple small building blocks. Additionally, many architectures allow the LUTs to be used as small memories, referred to as distributed memories, a feature that often is complemented with larger, dedicated memory blocks. Figure 2 summarizes the strengths of each approach.

Attribute	CPLD	FPGA
High Pin-to-Pin Speed	✓	
Fast Wide Logic	✓	
High I/O to Logic Ratio	✓	
Instant-On	✓	✓*
Register Intensive		✓
Distributed & Embedded Memory		✓

* Only a limited number of FPGA architectures provide this, such as LatticeXP.

Figure 2 – Comparative Strengths of CPLD and FPGA Approaches

Issues For Solution Optimization

With neither of the two current programmable architectures offering an optimal approach to the bus bridging, interfacing and control application space, there is room for both improvement and innovation. Following is an examination of the requirements in more detail, and a discussion of some of the issues associated with optimizing a programmable logic solution for these key functions.

High-Speed

At the densities typically required for the bus bridge and interfacing functions, the speed of the Macrocell and its associated routing has not kept pace with implementation technology as fast as the LUT-based approach. As a result, both the LUT and Macrocell approaches yield similar performance at the 130nm node. From a speed perspective, therefore, an architecture optimized for these functions could utilize either the macrocell or LUT approach at 130nm.

Although independent of logic implementation, the availability of Phase Locked Loops is important to bridging and interfacing functions. PLLs allow clock edges to be moved to meet the critical set-up and clock-to-out times often associated with bus interfaces. Clearly, the availability of this capability would be beneficial for devices targeting these applications.

Instant-on

Typically, bus interface and bridging functions, along with control logic, have to be operating ahead of other chips in the system. CPLDs, with their on-chip Flash or EEPROM technologies, satisfy this requirement. The vast majority of FPGAs, however, use SRAM technology, which requires a configuration to be loaded from an external, non-volatile memory at power-up. Such a configuration typically requires in the order of 100ms to complete. Clearly, an optimized solution will employ a non-volatile approach.

Upgradability

For over 10 years, designers who utilize programmable logic have enjoyed the capability to upgrade their designs in the field, providing significant flexibility for bug

fixes, response to standard changes and the need to add features and capabilities after manufacture. However, because most programmable logic devices let their I/O float during the load of a new configuration, it typically has been necessary to place the system in an offline mode prior to the logic update. However, for an increasing number of markets such as communications, networking and high-end computing, demands for extremely high system availability are making this approach less and less acceptable. A better solution is required.

High Logic to I/O Ratio

FPGAs typically have relatively complex I/O cells and support a broad range of I/O standards. Coupled with the practice of pitching the I/O to the core logic array limits the number of I/O that can be provided for smaller density devices. CPLDs, on the other hand, typically have streamlined I/Os supporting only the key I/O standards, and optimally arrange I/O independent of the core logic. In order to achieve the high I/O to logic ratio required, it is apparent that a next generation device should adopt the CPLD approach for its I/Os.

Flexible Data Buffering

Small data buffers are prevalent in bus bridging and interfacing applications. Traditionally these have been implemented in the registers associated with the Macrocell or LUT used for logic implementation. But this practice consumes significant resources. Adopting a LUT-based approach that allows distributed memory provides an elegant solution, implementing these memories with up to 16X the efficiency of approaches that do not implement distributed memory. This is illustrated in Figure 3.

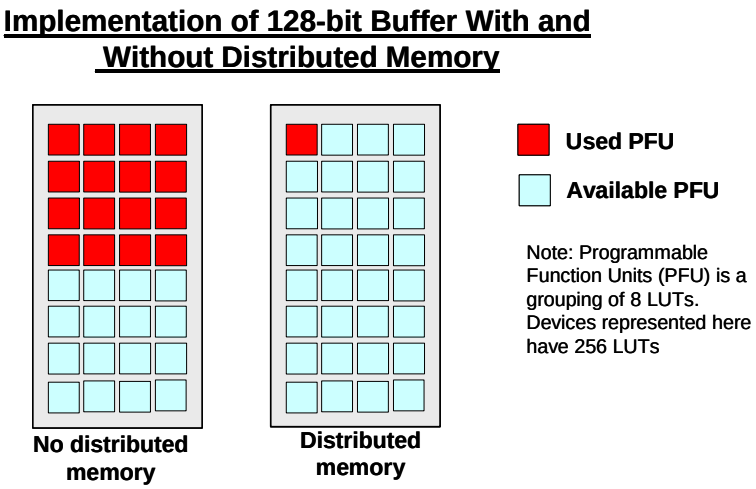


Figure 3 -- Distributed Memory Allows 16X Efficiency Improvement In Buffer Implementation

Low Power

A low power standby mode is increasingly commonplace and, for some battery-operated equipment, it is mandatory. While this need has been met by "zero power" versions of CPLDs, the same capability has not been provided to by reprogrammable FPGAs. Such a feature would expand the market applicability of next generation devices optimized for bus-interface, bridging and control applications.

MachXO Crossover Programmable Logic Devices

Lattice Semiconductor has developed a new class of programmable logic, Crossover Programmable Logic Devices, to better satisfy the needs of high-capacity CPLD and low-capacity FPGA users. The architecture of these devices blends CPLD and FPGA attributes in a single device in order to optimally serve a wide variety of applications, including the common bus bridging, interfacing and control functions.

Non-Volatile and SRAM Memory

The MachXO devices have been developed using a 130nm Flash + SRAM technology. The small geometries of the circuit elements allow fast operation with pin-to-pin speed as fast as 3.5ns. The combination of Flash + SRAM on the same device provides

significant flexibility to address the needs for field upgrades of logic and instant-on operation.

SRAM configuration bits control the operation of the MachXO devices. At power-up these bits are loaded via the on-chip non-volatile memory, resulting in logic availability in less than 1ms after power up, meeting the requirements of applications requiring instant-on capabilities. Figure 4 shows the operation of the different memories within the MachXO devices.

During system operation, the Flash memory may be programmed in the background. During this programming, the device's logic continues to be controlled by the SRAM configuration bits. At a convenient time the new configuration can be loaded into the SRAM. This update of logic can be done using Lattice's unique TransFR technology, which allows users to control precisely the device's I/O and logic state during the logic update. This allows field updates without taking the system off-line.

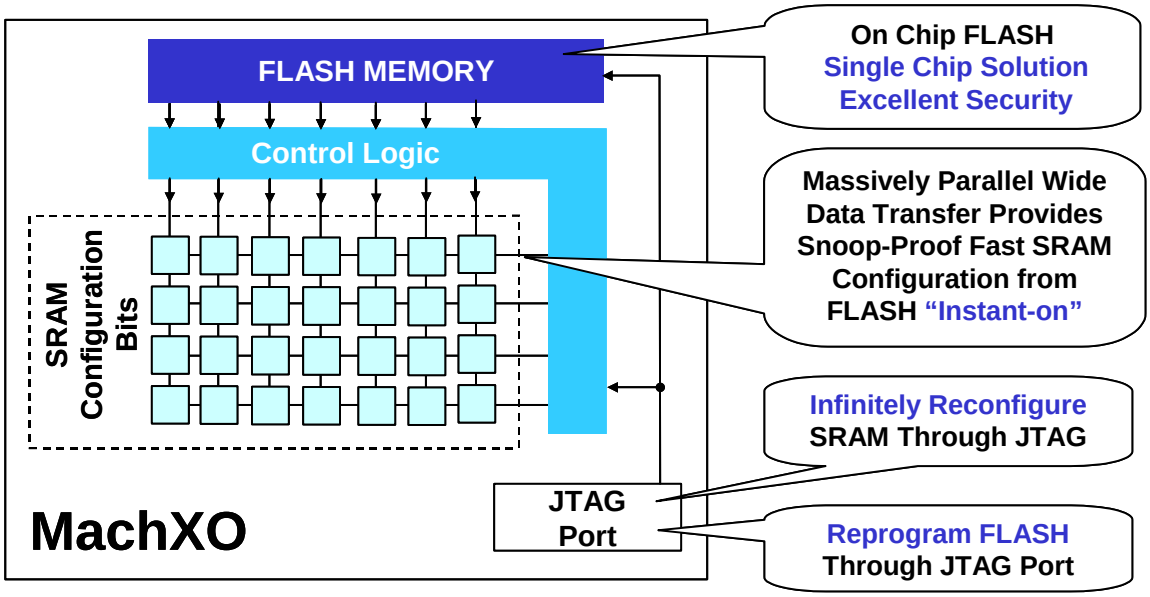


Figure 4 -- MachXO Configuration Memories

MachXO Architecture

At the core of the MachXO devices are Programmable Function Units (PFUs) that allow the implementation of logic and distributed memory. Logic is implemented using four

input LUTs, an approach that represents the de facto standard for the FPGA industry and is well understood by logic designers and logic synthesis tool suppliers.

The distributed memory capability provides an efficient and flexible method for implementing small data buffers. On the larger members of the MachXO family, to the left of the logic array, are blocks of sysMEM Embedded Block RAM (EBR), which provide 9kb memories for larger data buffers. Adjacent to the sysMEM blocks are sysCLOCK PLLs that provide designers the ability to adjust clock edges and synthesize new clocks as required.

Around the periphery of the devices, between 78 and 271 sysIO interfaces allow the device to interface with LVCMOS 3.3/2.5/1.8/1.5/1.2 and LVTTL. The I/O buffers have programmable drive strength, slew rate and input pull-up/pull-down arrangements to maximize flexibility when integrated with the rest of the system. The larger devices in the family also provide LVDS and PCI capability for further flexibility. Figure 5 illustrates the device architecture.

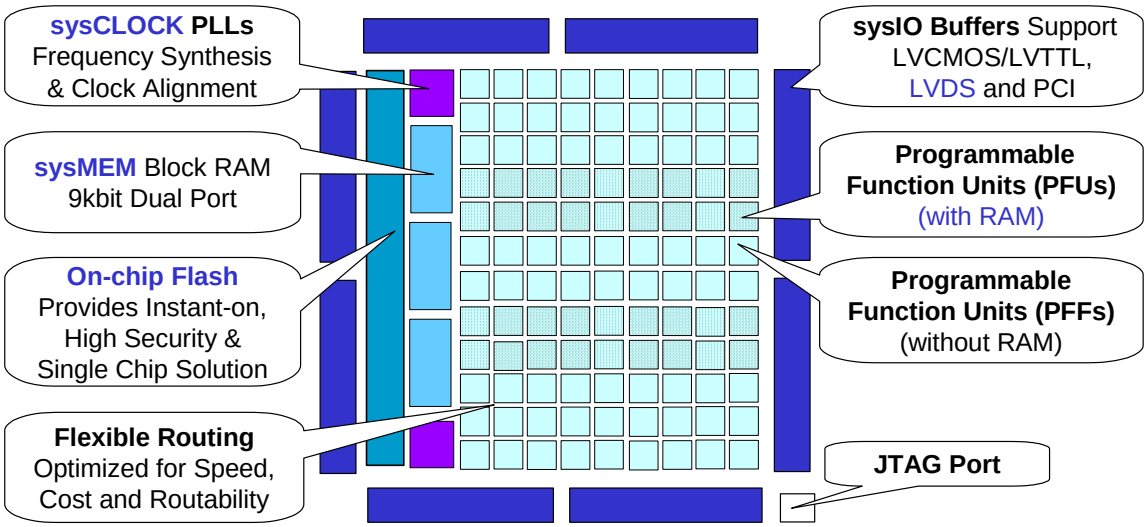
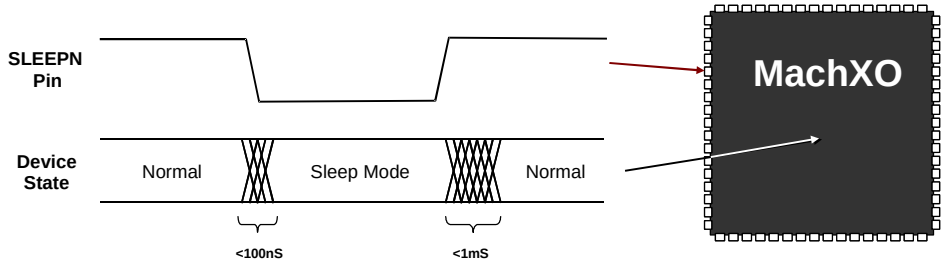


Figure 5 -- MachXO Architecture

Sleep Mode

The MachXO devices have a low power Sleep mode to address systems that have a low power standby state. In Sleep mode, the static power consumption of the MachXO

devices is reduced by over two orders of magnitude, to less than 100uA. Entry and exit to Sleep mode is controlled by a single SLEEPN pin, illustrated in Figure 6.



	Mode		
Characteristic	Normal	Off	Sleep
SLEEPN Pin	**High**	**X**	**Low**
Static Icc	**Typically <10mA**	**0**	**Typically <100uA**
Power Supplies	**Normal Range**	**Off**	**Normal Range**
Logic Operation	**User Defined**	**Non Operational**	**Non Operational**
I/O Operation	**User Defined**	**Tri-State**	**Tri-State**

Note: Sleep Mode is only available on 1.8/2.5/3.3V "C" version

Figure 6 -- MachXO Sleep Mode

Device Family

The MachXO family provides four logic capacities between 256 and 2280 LUTs and 78 to 271 I/O in a variety of popular packages. All devices in the same package are pin out compatible, allowing device capacity to be easily adjusted to match changing design requirements without re-laying out the circuit board. The devices are available in two power supply options, one supporting 3.3/2.5/1.8-volt operation and the other supporting 1.2-volt operation. The higher voltage version allows designers to benefit from the lower power, higher speed and low cost of 130nm technology without migrating to lower power supply voltages. Table 1 shows the different devices available in the MachXO family.

Device	MachXO 256	MachXO 640	MachXO 1200	MachXO 2280
LUTs	256	640	1200	2280
Distributed RAM (KBits)	2	6.1	6.4	7.7
EBR SRAM (KBits)	0	0	9.2	27.6
# EBR SRAM Blocks (9Kb)	0	0	1	3
V_{CC} Voltage	1.2/1.8/2.5/3.3V			
Number of PLLs	0	0	1	2
Max I/O	78	159	211	271
Packages:				
100-TQ (14X14)	78	74	73	73
144-TQ (20X20)		113	113	113
csBGA 100 (8X8)	78	74		
csBGA 132 (8X8)		101	101	101
ftBGA 256 (17X17)		159*	211	211
ftBGA 324 (19X19)				271
Samples	Now	Now	Q4	Q4
Production	Q3	Q3	Q4	Q1 06

* Initially fpBGA

Table 1 – MachXO Family Members

Summary

To date, neither high-capacity CPLDs nor low-capacity FPGAs have provided an optimal solution for implementation of the bus bridging, interfacing and control functions that are found in most systems. With the MachXO devices, Lattice has utilized a 130nm Flash and SRAM process to create a family of devices that combines the positive attributes of both approaches, providing an optimal solution to implementing these functions.

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