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EXAR'S ST16C654 AND XR16C854 COMPARED WITH TI'S TL16C754B

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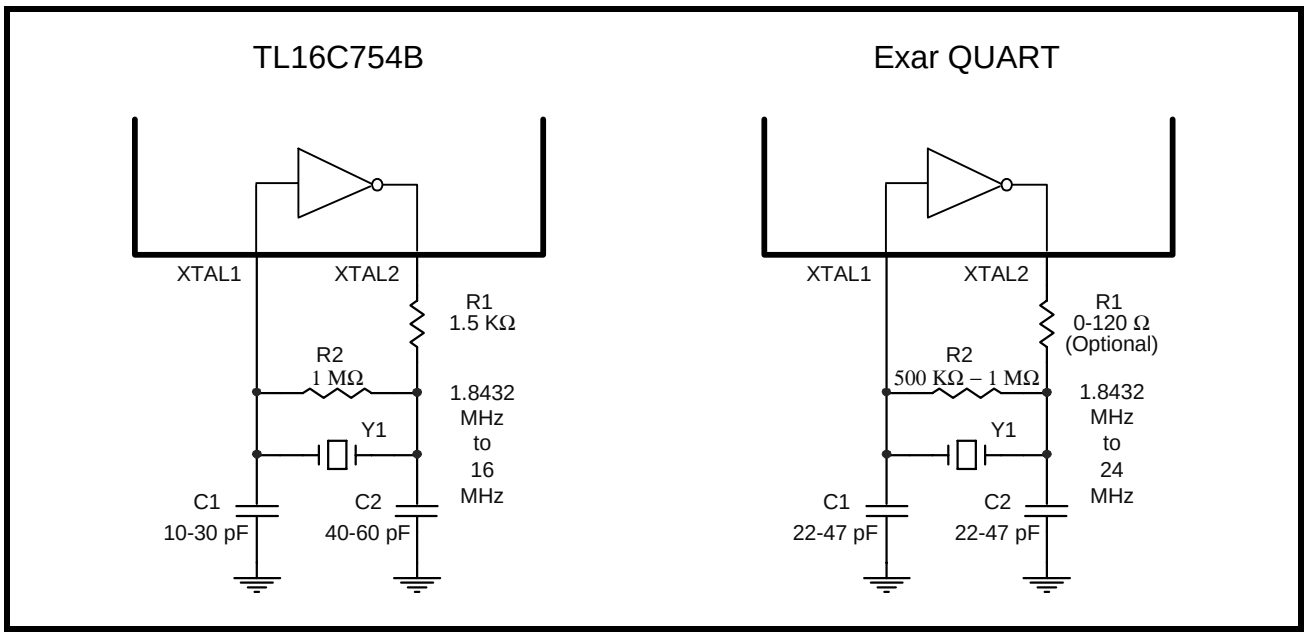
1.0 INTRODUCTION

This application note describes the major difference between Exar's ST16C654 and XR16C854 with TI's TL16C754B. These devices are similar, with a few hardware, bus timing and firmware-related differences.

1.1 HARDWARE DIFFERENCES

- The TI TL16C754B and Exar's ST16C654 and XR16C854 are all available in the 68-pin PLCC package. The Exar QUARTs are also available in the 64-pin TQFP and 100-pin QFP packages while the TI QUART is available in a 80-pin QFP package. The Exar and TI QUART are pin-to-pin compatible in the 68-pin PLCC package.
- The oscillator circuitry is similar, but there are some differences when using a crystal oscillator and when using an external clock. See Figure 1below for the differences in the oscillator circuitry for a crystal oscillator. When using an external clock input for frequencies greater than 24 MHz, the Exar QUARTs will require a 2K pull-up resistor on the XTAL2 pin.

FIGURE 1. CRYSTAL OSCILLATOR CIRCUITRY DIFFERENCES



1.2 BUS TIMING DIFFERENCES

- The TL16C754B requires that the -CS pin is asserted first before the -IOR or -IOW pin and the -IOR or -IOW pin must be de-asserted before the -CS pin is de-asserted. During a read, the Exar DUARTs can have either the -CS or the -IOR signal asserted first and have either signal be de-asserted first. The signals are wire-ORed in the Exar DUARTs, therefore the second signal asserted will initiate the read cycle and the first signal de-asserted terminates the read cycle. The same is true during a write for -CS and -IOW. The flexibility of the Exar DUARTs timing can be important in DSP, ARM, and MIPS designs.

1.3 Firmware Differences

1.3.1 Firmware Differences Between the ST16C654 and TL16C754B

The internal registers in the ST16C654 and TL16C754B are similar but with some exceptions:

Table 1: ST16C654 and TL16C754B Register Set Differences

A2:A0	R/W	ST16C654	TL16C754B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = Infrared Mode Enable • Bit-2 = Reserved (RI# during Internal Loop-back)	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	N/A	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	N/A	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A-D • Status Bits - RX FIFO level above RX Trigger Level for channels A-D
-FSRS pin asserted (100 pin package only)			
XXX	R	**FIFO Ready Register (FIFORdy)** • Values of RXRDY# A-D and TXRDY# A-D pins	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.1.1 Summary of Differences Between the ST16C654 and TL16C754B

The differences between the ST16C654 and TL16C754B is summarized in the table below.

TABLE 2: DIFFERENCES BETWEEN EXAR'S ST16C654 WITH TI'S TL16C754B

COMPARISON	ST16C654	TL16C754B
Data Bus Standard	**Intel or Motorola**	Intel
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**3 mA @ 3.3 V** **6 mA @ 5 V**	40 mA @ 3.3 V 50 mA @ 5 V
Max Frequency on XTAL1	16 MHz @ 3.3 V 24 MHz @ 5 V	**35 MHz @ 3.3 V** **50 MHz @ 5 V**
Data Sampling Rates	16X	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	1 Mbps @ 3.3 V 1.5 Mbps @ 5 V	**2.1875 Mbps @ 3.3 V** **3.125 Mbps @ 5V**
Package	68-PLCC, 64-TQFP, 100-QFP	68-PLCC, 80-PQFP
Operating Temperature Ranges	Commercial and Industrial	Industrial Only
TX/RX FIFO Size	64	64
TX/RX Trigger Tables	1 Trigger Table	**2 Trigger Table**
TX FIFO Interrupt Trigger Levels	4 Selectable	**16 Selectable**
RX FIFO Interrupt Trigger Levels	4 Selectable	**16 Selectable**
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	Auto Xon/Xoff Flow Control	Auto Xon/Xoff Flow Control
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	Sleep Mode with Auto Wake-up	Sleep Mode with Auto Wake-up
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	N/A	N/A

1.3.2 Firmware Differences Between the TL16C754B and XR16C854

The internal registers in the XR16C854 offers more features than the TL16C754B with some differences:

TABLE 3: XR16C854 AND TL16C754B REGISTER SET DIFFERENCES

A2:A0	R/W	XR16C854	TL16C754B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = IR Mode Enable • Bit-2 = OP1 Control/Auto RS485 Enable	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	N/A	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	N/A	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A and B • Status Bits - RX FIFO level above RX Trigger Level for channels A and B
LCR Bit-7 = 0, FCTR Bit-6 = 1			
111	W	**Enhanced Mode Select Register (EMSR)** • RX/TX DMA Select, FLVL select - TX or RX FIFO	N/A
111	R	**FIFO Level Register (FLVL)** • Current Level of the TX or RX FIFO	N/A
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	**Device Revision (DREV)**	N/A
001	R	**Device ID (DVID)**	N/A
LCR = 0xBF			
000	R	**FIFO Data Count Register (FC)**	N/A
000	W	**Trigger Level Register (TRG)** • Programmable Trigger Levels 1-64 for TX and RX FIFO	N/A
001	R/W	**Feature Control Register (FCTR)** • RX/TX Programmable Trigger Level Select, Scratchpad Swap, Trigger Table Select, Auto RS485 Enable, RX IR Input Inversion, Auto RTS Hysteresis Select (LSB)	N/A
-FSRS pin asserted (100 pin package only)			
XXX	R	**FIFO Ready Register (FIFORdy)** • Values of RXRDY# A-D and TXRDY# A-D pins	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.2.1 Summary of Differences Between the XR16C854 and TL16C754B

The differences between the XR16C854 and TL16C754B is summarized in the table below.

TABLE 4: DIFFERENCES BETWEEN EXAR'S XR16C854 WITH TI'S TL16C754B

COMPARISON	XR16C854	TL16C754B
Data Bus Standard	**Intel and PC Mode**	Intel
Device ID and Revision	**Device ID and Revision**	N/A
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**2.7 mA @ 3.3 V** **4 mA @ 5 V**	40 mA @ 3.3 V 50 mA @ 5 V
Max Frequency on XTAL1	22 MHz @ 3.3 V 33 MHz @ 5 V	**35 MHz @ 3.3 V** **50 MHz @ 5 V**
Data Sampling Rates	16X	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	1.375 Mbps @ 3.3 V 2 Mbps @ 5 V	**2.1875 Mbps @ 3.3 V** **3.125 Mbps @ 5V**
Package	68-PLCC, 64-TQFP, 100-QFP	68-PLCC, 80-PQFP
Operating Temperature Ranges	**Commercial and Industrial**	Industrial Only
TX/RX FIFO Size	**128**	64
TX/RX Trigger Tables	**4 Trigger Tables**	2 Trigger Table
TX FIFO Interrupt Trigger Levels	**Programmable (Table D)** 4 Selectable (Tables A-C)	16 Selectable
RX FIFO Interrupt Trigger Levels	**Programmable (Table D)** 4 Selectable (Tables A-C)	16 Selectable
TX/RX FIFO Counters	**TX/RX FIFO Counters**	N/A
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	Auto Xon/Xoff Flow Control	Auto Xon/Xoff Flow Control
Auto Hysteresis Level	16 Selectable Levels	16 Selectable Levels
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	Sleep Mode with Auto Wake-up	Sleep Mode with Auto Wake-up
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	**Auto RS485 Mode**	N/A

1.4 REPLACING THE TL16C754B WITH THE ST16C654 OR XR16C854

You can directly replace TI's TL16C754B with ST16C654 or XR16C854 with minimal hardware changes if using the 68-PLCC package. The crystal oscillator circuitry should work in most cases, but it may be necessary to modify the oscillator circuitry as shown in Figure 1. If replacing with the 64-TQFP or 100-QFP packages, hardware changes will be required since the TL16C754B is not available in that package.

Replacing the TL16C754B with the ST16C654 is simple if not using the Automatic RTS/CTS Flow Control and hysteresis levels. The software will need to be updated if using Infrared Mode with the ST16C654.

When replacing the TL16C754B with the XR16C854, the software will need to be updated in order to take advantage of the enhanced features of the XR16C854 that are not available or different in the TL16C754B.

There should not be any timing problems replacing the TL16C754B with the ST16C654 or XR16C854 because they are more flexible than the TL16C754B as described in the bus timing section.

1.5 TL16C754B KNOWN DEFICIENCY

The TL16C754B has a known deficiency and is directly stated in TI's datasheet, but TI does not have any plans to fix them.

On page 13 of the TL16C754B's datasheet dated "November 1999," TI gives a note advising not to write to Baud Rate Divisors DLL and DLH (DLM) while in sleep mode. Exar QUARTs do not have any such problems.